REMARKS

Claims 2-7 and 9-33 are pending in this application. Claims 2-5 and 9-19 have been amended by this Amendment. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

The Office Action dated January 28, 2002 entered a restriction requirement between Group I consisting of claims 1-21 and 23-33 and Group II consisting of claim 22, and rejected claims 2-7, 9-21 and 23-33 as being obvious over a combination of a number of different references.

Restriction Requirement

The restriction requirement is set forth in parts 1-3 on pages 2-3 of the Office Action. Reconsideration and withdrawal of the restriction requirement is respectfully requested.

It is respectfully submitted that the amended device claims 2-7, 9-21 and 23-33 and method claim 22 are very closely related to one another, to the point of justifying a common examination. Comparing the device claims, as amended, with method claim 22, for example, it is noted that both the device claims and the method claim are directed to pyramidal bump electrodes formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane. The amended device claims include specific

method features concerning the bonding operation. As such, numerous common issues will be raised between the amended device claims and the method claim during the examination, both in terms of searching and consideration by the Examiner.

Accordingly, it is respectfully submitted that the common issues of these claims call for a common examination of both the device and method claims in this application. Such a common examination will avoid redundant efforts in searching and prosecuting which will almost surely result if this restriction requirement is not removed.

Further, it is urged that such a common examination is warranted, notwithstanding the fact that other methods could possibly be used for manufacturing the device, as pointed out in the Office Action. MPEP 803 specifies:

> "If the search and examination of an entire application can be made without serious burden, the Examiner must examine it on the merits, even though it includes claims to distinct or independent inventions."

It is respectfully submitted that this is the situation here, given the close relationship between the device and the method claims in question. Accordingly, it is respectfully requested that the Examiner reconsider this restriction requirement in light of the above comments, and MPEP 803, and, correspondingly, remove the restriction requirement.

Finally, it is respectfully submitted that the Office Action fails to establish the distinctness between the process

of making and the product made in accordance with the requirements of MPEP 806.05(f). This section of the Manual states that a restriction between a process of making and a product made is permissible:

> "if the Examiner can demonstrate that the product as claimed can be made by another materially different process; defining the product in terms of a process by which it is made is nothing more than a permissible technique that applicant may use to define the invention."

It is respectfully submitted that the Office Action fails to demonstrate that the product as claimed can be made by another materially different process as required by MPEP 806.05(f). Accordingly, it is respectfully submitted that the statements made in the Office Action are insufficient to justify the restriction requirement.

Although the applicants believe that the restriction requirement is not warranted for the reasons set forth above, in order to be fully responsive to the restriction requirement, applicants hereby elect Group I claims 2-7, 9-21 and 23-33, drawn to the device, subject to the traverse provided herein.

Obviousness Rejection

The obviousness rejection relies upon a proposed combination of the second embodiment shown in Figs. 14A-14D of U.S. Patent No. 5,508,561 to Tago et al (this embodiment hereinafter being referred to simply as "Tago"), U.S. Patent

No. 6,049,130 to Hosomi et al, and the pyramid shape shown in Fig. 2 of Japanese Pat. 08191072. Applicants respectfully traverse the rejection at least because it fails to establish a prima facie case that the cited references suggest each and every one of the combination of features recited in the rejected claims.

The response to arguments on pages 12-13 again asserts that Hosomi et al teach "using pyramid shaped bumps using conventional thermal compression." Applicants respectfully disagree. In Hosomi, the bump 6 is not pyramidal. Although element 7 may be considered pyramidal, it is an inner lead rather than an electrode. Furthermore, the cited portion at col. 1, line 45, to col. 2 ,line 68, does not teach "using pyramid shaped bumps." Rather, it teaches a bonding method for more firmly bonding Au bumps to Cu leads.

The response to arguments also asserts that JP 08-191072 to Takahiro shows "a variety of shapes including triangular/conical/square shaped pyramidal bumps bonded onto pad electrodes." However, the parts that the rejection is apparently referring to is just printed adhesive resin and does not suggest the elements recited in the rejected claims.

Notwithstanding applicants' disagreement with the outstanding rejection, applicants have amended all of the rejected claims in attempt to distinguish over the cited references. Specifically, applicants have amended the claims to recite that the pyramidal bump electrodes "have a sharp

tip" and are formed of "etched pyramidal holes on a base material having a crystal orientation plane." Exemplary, non-limiting, support for the claim amendments can be found at page 13, lines 14-20, of the specification.

Applicants respectfully submit that the amended claims are allowable at least because the cited references fail to disclose or suggest a pyramidal bump electrode having a sharp tip. Furthermore, applicants submit that the amended claims are also allowable because the cited references fail to disclose or suggest a pyramidal bump electrode formed from etched pyramidal holes on a base material having a crystal orientation plane. Furthermore, applicants submit that the amended claims are also allowable because the cited references fail to disclose or suggest a pyramidal bump electrode formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit

account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.38090X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
Robert M. Bauer, Registration No. 34,487

RMB/kd
703/312-6600

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 2-5 and 9-19 have been amended as follows:

2. (Amended) A semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded through an anisotropic conduction film onto pad electrodes arranged on a semiconductor chip.

3. (Amended) A semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded by thermal compression onto pad electrodes arranged on a semiconductor chip.

4. (Amended) A semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded by thermal compression onto pad electrodes arranged on a semiconductor chip so that said pyramidal bump electrodes

and said pad electrodes can form an alloy at the junctions by said thermal compression.

5. (Amended) A semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded onto rewired metal conduction pads that are electrically connected to pad electrodes arranged on a semiconductor chip.

9. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded through an anisotropic conduction film onto pad electrodes arranged on a semiconductor chip, said mounting structure enabling said semiconductor device to be mounted on a substrate by respectively bonding said pyramidal bump electrodes onto terminals formed on said substrate.

10. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal

orientation plane, respectively bonded by thermal compression onto pad electrodes arranged on a semiconductor chip, said mounting structure enabling said semiconductor device to be mounted on a substrate by respectively bonding said pyramidal bump electrodes onto terminals formed on said substrate.

11. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded by thermal compression onto pad electrodes arranged on a semiconductor chip so that said pyramidal bump electrodes and said pad electrodes can form an alloy at the junctions by said thermal compression, said mounting structure enabling said semiconductor device to be mounted on a substrate by respectively bonding said pyramidal bump electrodes onto terminals formed on said substrate.

12. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded onto pad electrodes arranged on semiconductor chip, said mounting structure enabling said semiconductor device to be mounted on a

substrate by respectively soldering said pyramidal bump electrodes onto terminals formed on said substrate.

13. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded through an anisotropic conduction film onto pad electrodes arranged on a semiconductor chip, said mounting structure enabling said semiconductor device to be mounted on a substrate by respectively soldering said pyramidal bump electrodes onto terminals formed on said substrate.

14. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded by thermal compression onto pad electrodes arranged on a semiconductor chip, said mounting structure enabling said semiconductor device to be mounted on a substrate by respectively soldering said pyramidal bump electrodes onto terminals formed on said substrate.

15. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded by thermal compression onto pad electrodes arranged on a semiconductor chip so that said pyramidal bump electrodes and said pad electrodes can form an alloy at the junctions by said thermal compression, said mounting structure enabling said semiconductor device to be mounted on a substrate by respectively soldering said pyramidal bump electrodes onto terminals formed on said substrate.

16. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded onto pad electrodes arranged on a semiconductor chip, said mounting structure enabling said semiconductor device to be mounted on a substrate by respectively bonding said pyramidal bump electrodes onto terminals formed on said substrate and by bonding said semiconductor device to said substrate with an adhesive.

17. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded through an anisotropic conduction film onto pad electrodes arranged on a semiconductor chip, said mounting structure enabling said semiconductor device to be mounted on a substrate by respectively bonding said pyramidal bump electrodes onto terminals formed on said substrate and by bonding said semiconductor device to said substrate with an adhesive.

18. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded by thermal compression onto paid electrodes arranged on a semiconductor chip, said mounting structure enabling said semiconductor device to be mounted on a substrate by respectively bonding said pyramidal bump electrodes onto terminals formed on said substrate and by bonding said semiconductor device to said substrate with an adhesive.

19. (Amended) A mounting structure in a semiconductor device having a plurality of pyramidal bump electrodes with a

sharp tip, formed of conductive materials filling up etched pyramidal holes on a base material having a crystal orientation plane, respectively bonded by thermal compression onto pad electrodes arranged on a semiconductor chip so that said pyramidal bump electrodes and said pad electrodes can form an alloy at the junctions by said thermal compression, said mounting structure enabling said semiconductor device to be mounted on a substrate by respectively bonding said pyramidal bump electrodes onto terminals formed on said substrate and by bonding said semiconductor device to said substrate with an adhesive.